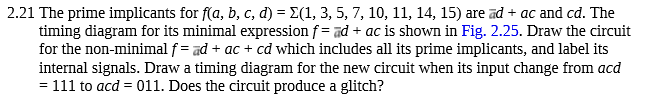
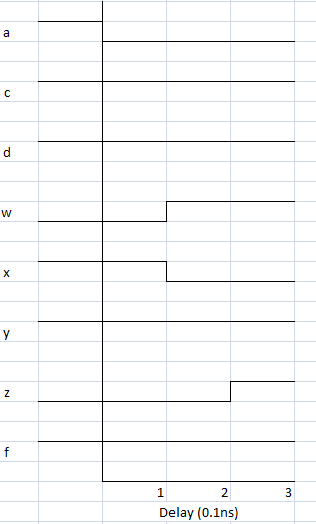
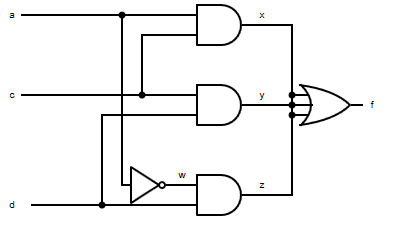
Austin Smothers

Professor Bustamante

CSC 137

Assignment 3

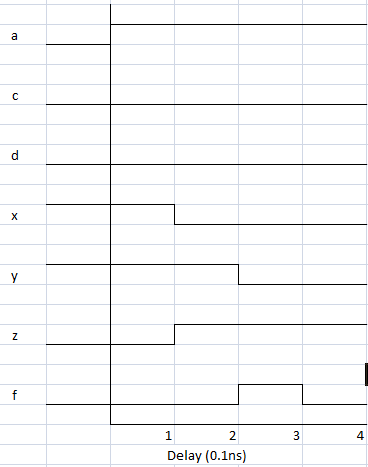
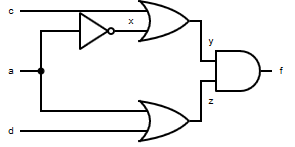




There is no glitch because the y circuit stays "on" the entire time (since c and d don’t change values). The result is that f is always "on".

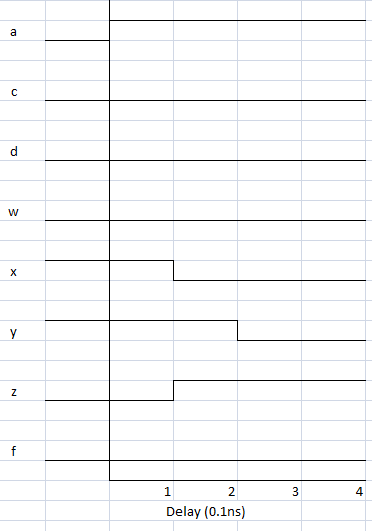
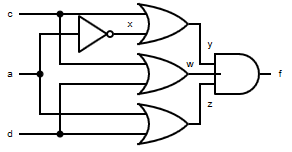




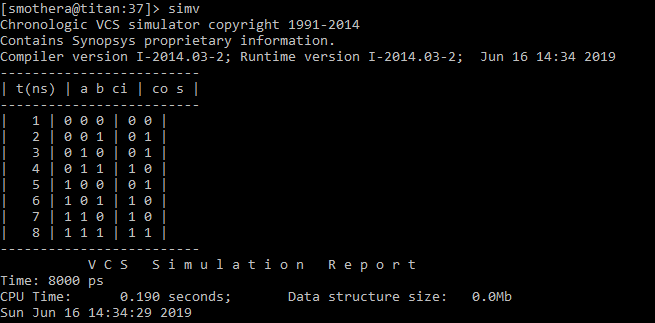


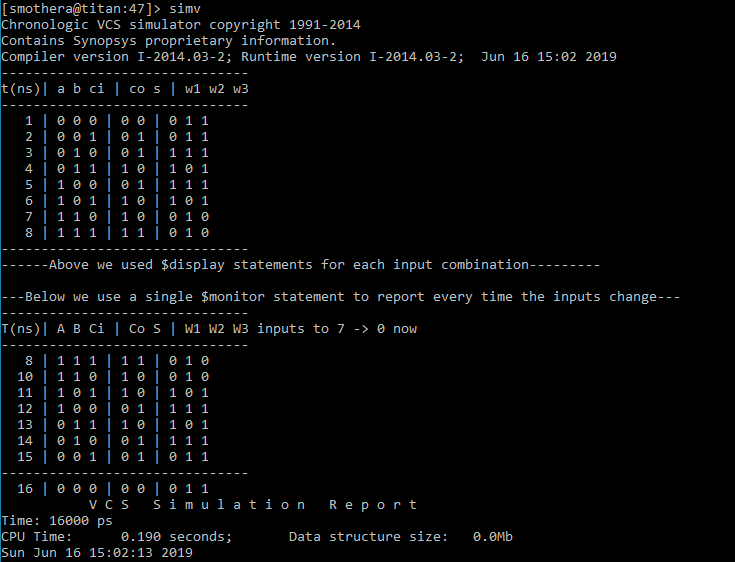
Yes there is a 0-hazard glitch, as y and z both briefly become 1, causing f to flip. Then y registers as 0, and f becomes 0, causing a glitch.





No, there are no hazards in this circuit.





3) How does full\_adder\_wires[\_tb].v Verilog circuit allow for the internal signals w1, w2, w3 to be visible on the test bench?

We declared the wires as parameters in the output portlist instead of in the "logic" file and then output them.